...when timing matters

M3027 Series
SPECIFICATION FOR 5.0x7.0mm LVCMOS SMT VCXO

FEATURES

LVCMOS Output
Low RMS jitter performance 12 kHz to 20 MHz
Low Phase Noise
Compliant to RoHS directive

APPLICATIONS

Base station controllers
4G/LTE applications
Ethernet, SyncE
Test and Measurement

Ordering Information:

Product Family	Temperature Range		Stability*	Enable/Disable		Absolute Pull Range (APR)		Logic Type		Package/Lead Configuration		Frequency
	Code	Value	Code	Code	Value	Code	Value	Code	Value	Code	Value	
M3027	**2** **6**	-40 °C to +85 °C -20 °C to +70 °C	**0**	**T** **V**	Enable High (pad 2) No Enable/Disable	**G** **C** **F**	±20 ppm ±25 ppm ±40 ppm	**C**	LVCMOS	**N**	Leadless	XXX.XXXX MHz
Example: M302720VGCN 122.8800 MHz												
M3027	**2**		**0**	**V**		**G**		**C**		**N**		**122.8800MHz**

* Stability is included in the APR specification.

Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F_O	1		170	MHz	
Frequency Stability						
Frequency Stability	ΔF/F	See ordering information				
Aging		-5		+5	ppm	1st year
		-3		+3		Per year thereafter
RF Output						
Output Type		CMOS				
Output Load		15 pF CMOS load				
Symmetry (duty cycle)	T_{DC}	45		55	%	@ 50% Vdd
Logic "0" Level	V_{OL}			10% Vdd	V	
Logic "1" Level	V_{OH}	90% Vdd			V	
Rise/Fall Time	T_R/T_F			5.0	ns	1.000000 – 50.000000 MHz
10% Vdd to 90% Vdd				3.0		50.000001 – 170.000000 MHz
Start-up Time	T_{SU}			10	ms	$T_{ambient}$ = +25°C
Enable Logic (Pad 2)		70% V_{CC} or N/C			V	Output Enabled
Disable Logic (Pad 2)				30% V_{CC}	V	Output Disabled to high-Z
Frequency Adjustment						
Control Voltage		0.30	1.65	3.00	V	Pad 1
Absolute Pull Range	APR	See ordering information				
Modulation Bandwidth	f_m	10			kHz	-3 dB
Input Impedance	Z_{in}	50			kΩ	Pad 1
Linearity				10	%	
Supply Voltage & Power Consumption						
Operating Voltage	V_{CC}	3.135	3.300	3.465	V	
Supply Current	I_{CC}			20	mA	1.000000 – 50.000000MHz
				30		50.000001 – 100.000000MHz
				50		100.000001 – 170.000000MHz
Other Parameters						
Phase Jitter (RMS)	ΦJ			0.4	ps	12kHz to 20MHz @ 122.88MHz

Revision 0
10/15/15

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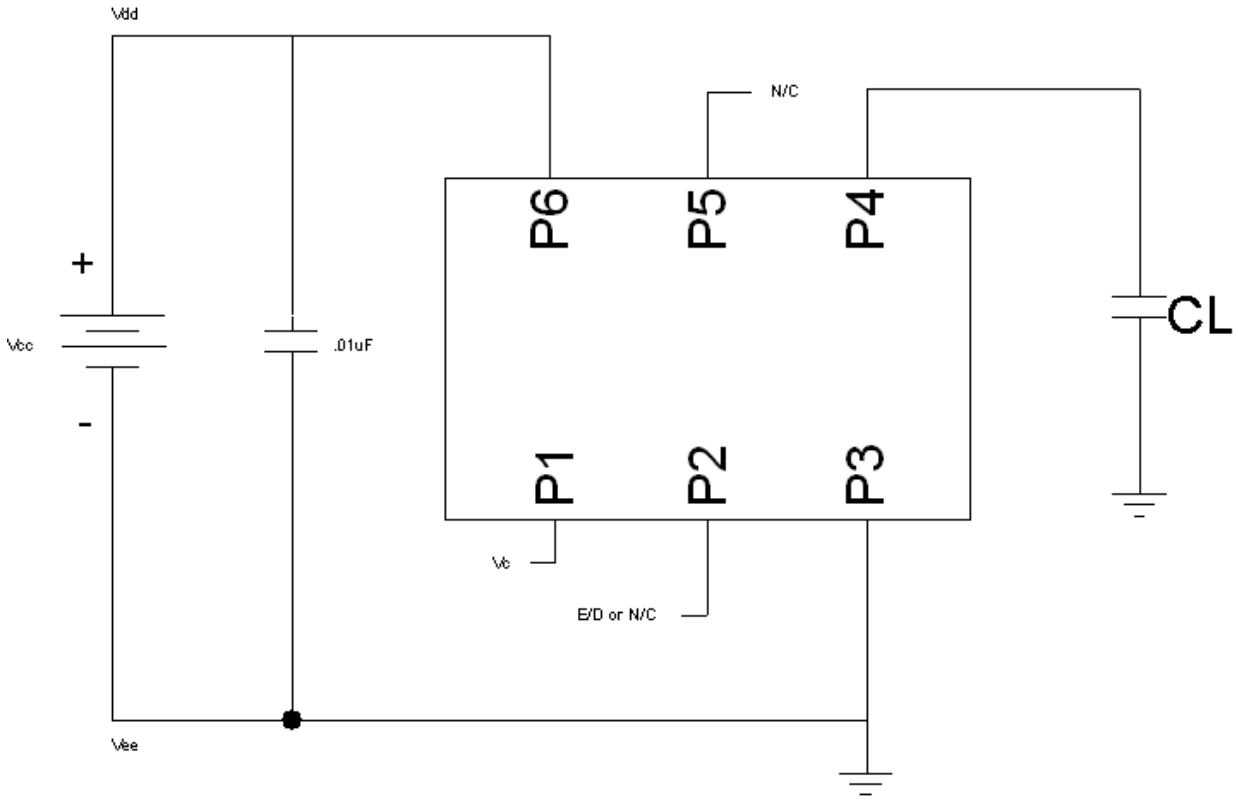
Environmental & Packaging Requirements:

Operating Temperature	T_A	See ordering information			°C	
Storage Temperature	T_S	-55		+125	°C	
Mechanical Shock	Per MIL-STD-202, Method 213, Condition E					
Vibration	Per MIL-STD-202, Method 204D, Condition D					
Aging	+85°C ±3°C, 720H (No BIAS)					
Humidity	+40°C ±2°CX90~95%, 96H (NO BIAS)					
Thermal Cycle	Per MIL-STD-883, Method 1011, Condition A					
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10^{-8} atm cc/s of Helium)					
Moisture Sensitivity Level	MSL1					
Solderability	Per EIAJ-STD-002, Method 208					
Max. Soldering Conditions	See solder profile, Figure 1					
Pad Termination	Gold, 1 µm maximum thickness					
Package Type	6-pad 5.0 X 7.0 mm leadless ceramic. RoHS compliant.					

Typical LVCMOS Test Circuit & Load Circuit Diagrams:



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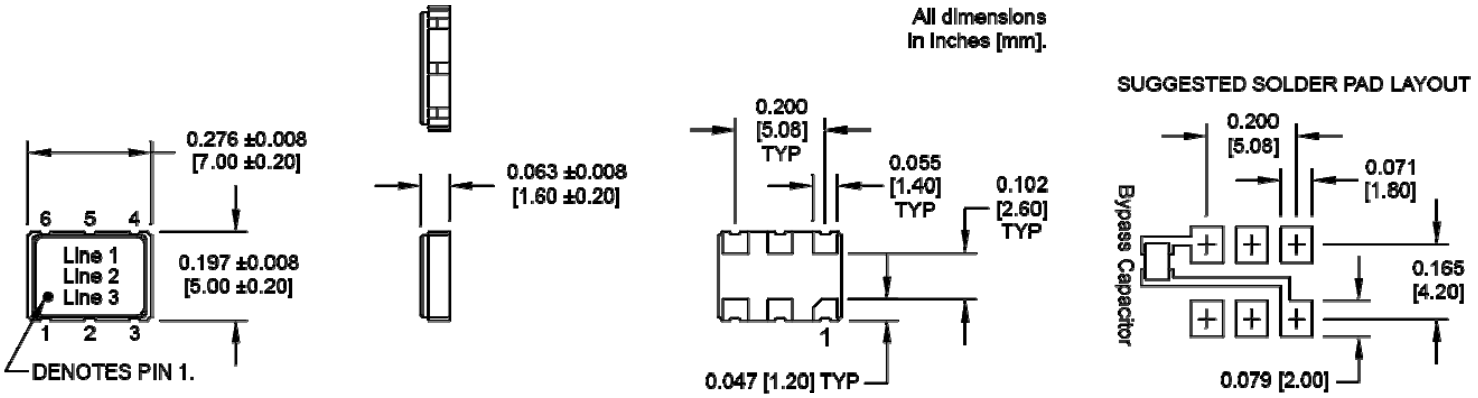
Marking, Pin Out:

Pad	Function
1	Control Voltage
2	Enable/Disable or N/C
3	Ground
4	Output
5	N/C
6	$+V_{CC}$

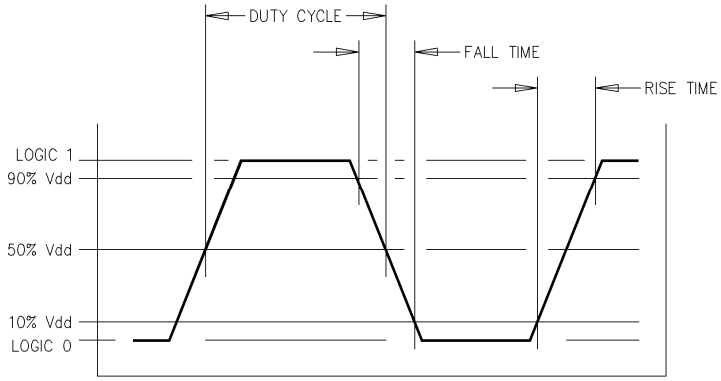
Part Marking	
Line 1	[part designation]
Line 2	FFFMFFFF
Line 3	M yy ww vv

Legend	
M	MtronPTI
F	Frequency
yy	Year
ww	Work Week
vv	Factory code

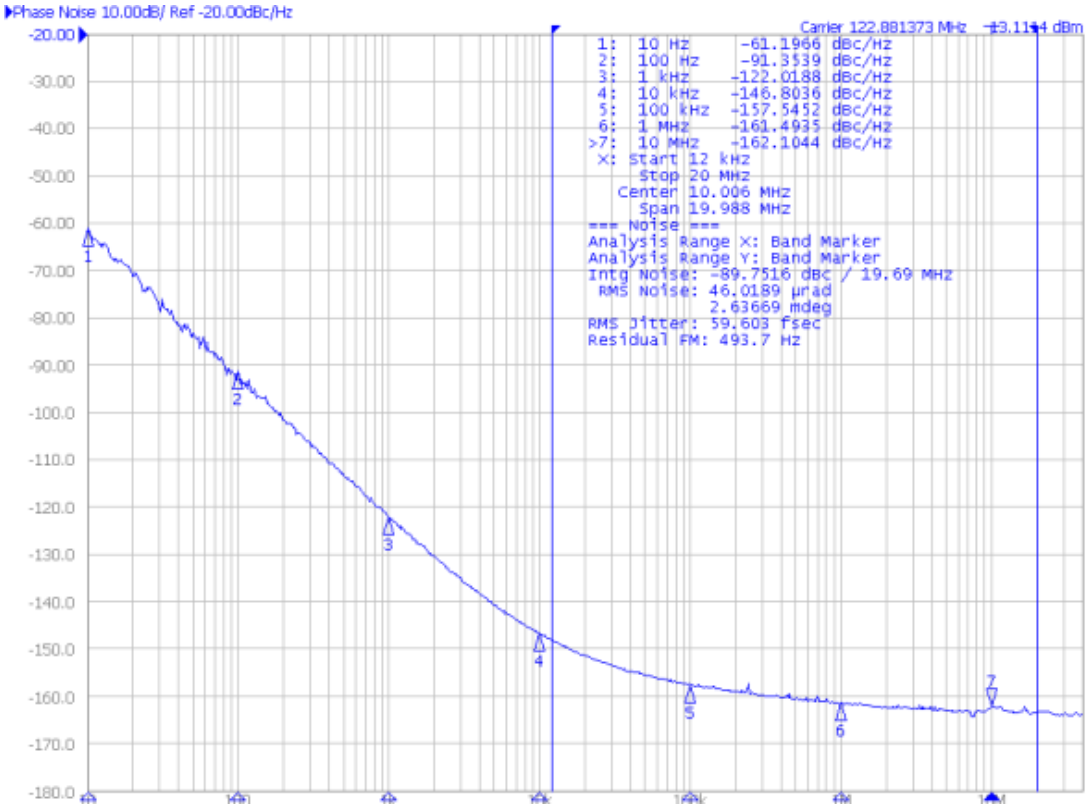
Dimensions:



Output Waveform:



LVCMOS Phase Noise Plot:



Soldering Conditions:

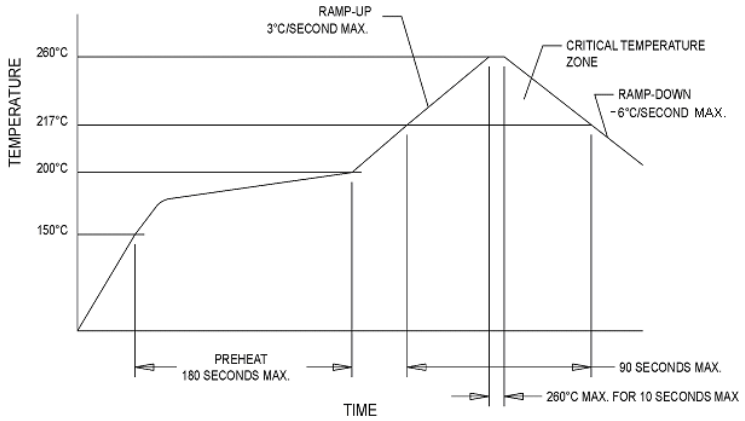
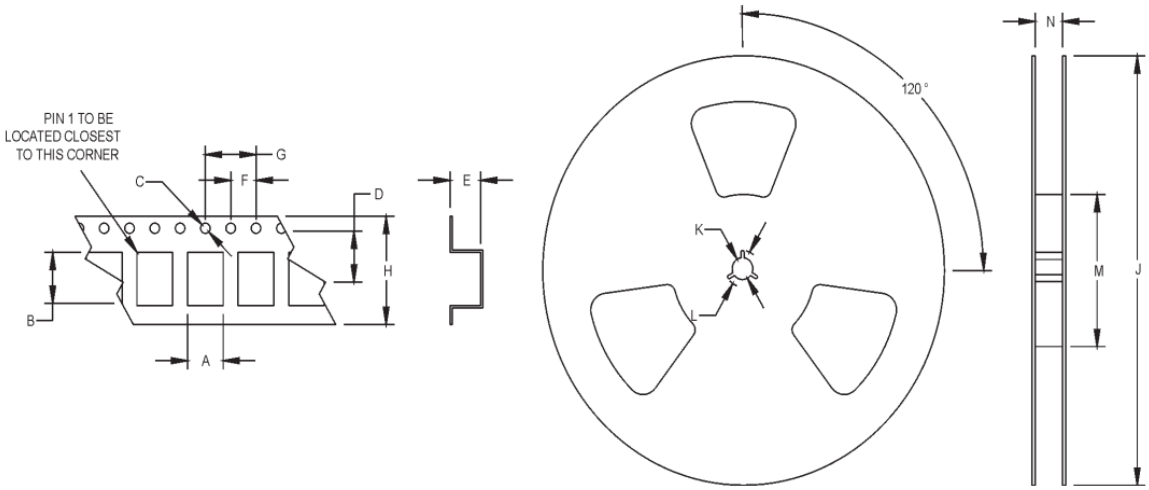


Figure 1

Tape and Reel Specifications:

All units in mm



Tape and Reel Specifications											
A	B	C	D	E	F	G	H	J	K	L	M
5.32	7.28	1.5	7.5	2.2	4	8	16	178	13.5	24.8	80